Cellular Monte Carlo Modeling of $Al_xIn_{1-x}Sb$/InSb Quantum Well Transistors

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Summary. In this work, an Indium Antimonide (InSb) quantum well transistor is investigated using full-band Monte Carlo simulations. The steady-state characteristic of the device is first analyzed, showing particle transport along a two-dimensional electron gas (2DEG). The small-signal behavior of the device is also investigated. Finally, a noise analysis is performed, allowing for a two-dimensional mapping of the noise within the device.

1 Introduction

Due to its low band gap and high electron mobility, Indium Antimonide (InSb) is a promising material for extremely high frequency devices operating at low voltages [1]. Although these desired properties are not easily accessible at room temperature, techniques based on minority-carrier exclusion and extraction [2] have been used to raise the device operating temperature, allowing for room temperature operation of InSb MISFETs [3]. More recently, AlInSb/InSb quantum well transistors have been developed [4]. The purpose of this work is to investigate the static and dynamic behaviour of these devices using full-band Monte Carlo simulations.

2 Cellular Monte Carlo Simulations

The full-band particle-based simulation tool used for modeling the devices is the Cellular Monte Carlo (CMC) [5]. InSb bulk simulations have been performed at 77K for benchmarking purposes. The results are compared to published data [6,7] in Fig.1 (a) and (b), showing the electron drift velocity and energy versus the ‹100› electric field, respectively. Good agreement is observed.

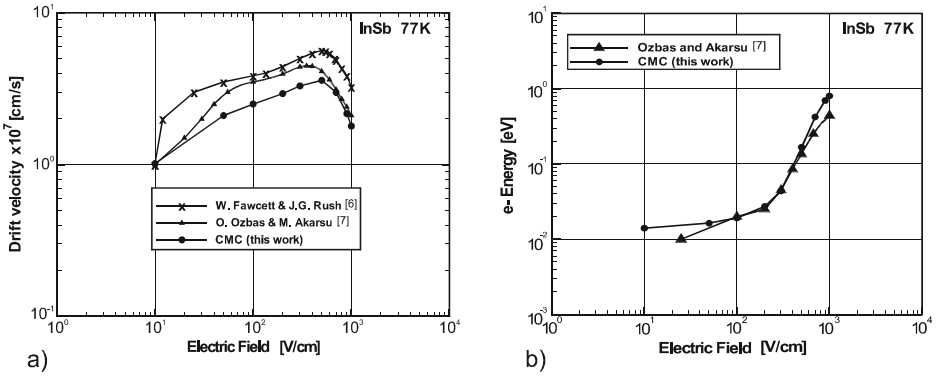

Fig. 1. Electron drift velocity (a) and energy (b) obtained with CMC simulations and compared to other published results [6,7].

3 AlInSb/InSb Quantum Well Transistor

The cross section of the AlInSb/InSb quantum well transistor is shown in Fig.2 (a). A 15 nm layer of doped $Al_{0.3}In_{0.7}Sb$ is separated from a 20 nm conducting InSb channel by a 5 nm $Al_{0.3}In_{0.7}Sb$ spacer. The 200 nm $Al_{0.3}In_{0.7}Sb$ substrate underneath is unintentionally doped. To account for the quantization of the electron motion in the vicinity of the heterojunction, the effective potential approach [8] has been used.

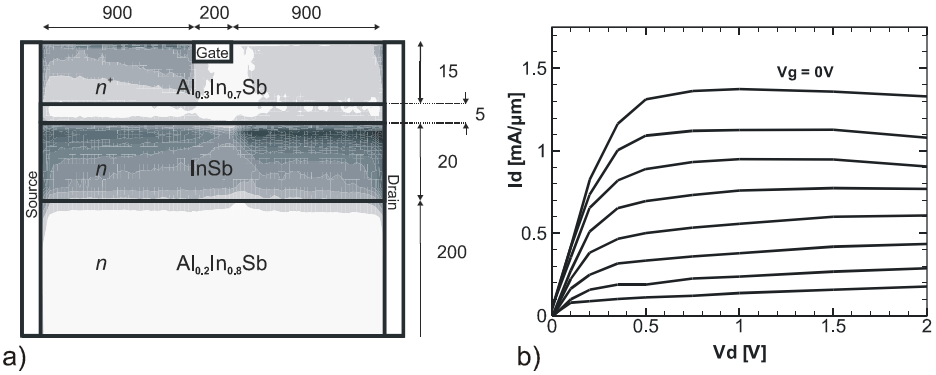

Fig. 2. (a) 2D schematic layout of the simulated device. (b) Drain current-voltage characteristics. The gate biases are applied every 0.1 V.

Fig.2 (b) shows the drain current versus the drain voltage for gate biases ranging from -0.7 V to 0 V. The knee voltage is observed at 0.5 V. The device exhibits good saturation characteristics, and a slight decrease in the drain current can be observed for drain voltage greater than 1 V. This negative differential

resistance has already been observed in InSb structures and reported in literature [6].

4 Results

The frequency analysis is performed using both a Fourier decomposition technique [9] and monochromatic sinusoidal [10]. An average of 200,000 particles has been simulated to model the electron population. Typical simulated times range from a few picoseconds to over a hundred picoseconds, averaging to 77 minutes of CPU time per simulated picosecond on a Pentium IV 2.4 GHz processor.

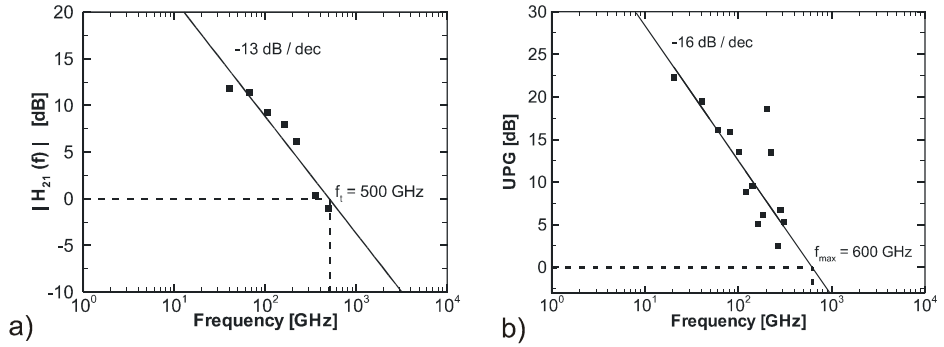

Fig. 3. Short circuit current gain (a) and unilateral power gain (b) as a function of frequency.

The short circuit current gain h_{21} and the unilateral power gain UPG are shown as a function of frequency on Fig.3 (a) and (b), respectively. A linear fit is indicated with a solid line, showing a slope of 13 and 16 dB per decade, respectively. A cutoff frequency f_T = 500 GHz and a maximum frequency of oscillation f_{max} = 600 GHz are extrapolated, and the f_T/f_{max} ratio of 1.2 is in good agreement with published results [4]. The frequencies reported here are larger than the experimental ones; however, they correspond to internal small-signal values without consideration of any contact and connector resistance and capacitance, which typically have a negative impact on the device performance. Moreover, the magnitudes of the voltage perturbations used here are on the border of small-signal analysis, to minimize the impact of noise on the results. Longer simulations with a larger number of particles would reduce the noise, allowing for smaller perturbation amplitudes and resulting in a more accurate estimation of the frequencies. Finally, the calculated gate delay CV/I = 0.87 ps is found to be close to the experimental value of 1.06 ps reported in [4].

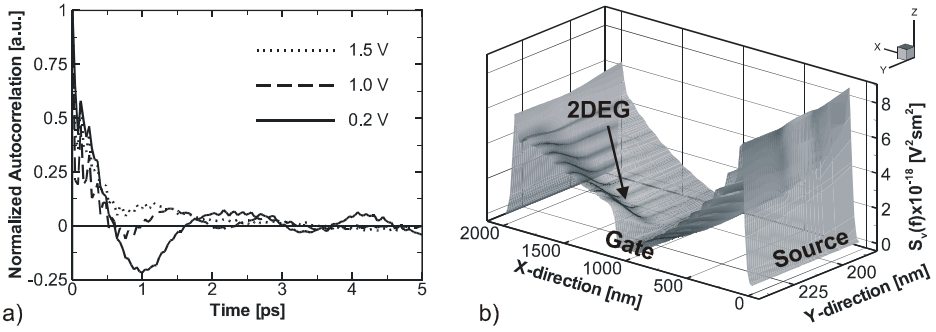

Fig. 4. (a) Voltage autocorrelation function, along a section below the gate. (b) Voltage PSD at 100 GHz as a function of position in the device.

For the noise analysis, the voltage fluctuations about steady state are analyzed in the time domain through calculation of the respective autocorrelation functions, and in the frequency domain through their Fourier transforms yielding their Power Spectral Density (PSD) [11]. The autocorrelation function of the voltage fluctuations is shown in Fig.4(a), along a 2D slice underneath the gate region, for three drain voltages. After an exponential decay corresponding to the dielectric relaxation time, diminishing oscillations are observed. They are attributed to the concurrent contributions of plasma frequency oscillations and dielectric relaxation [11]. These oscillations tend to disappear as the applied bias is increased, and the negative tail directly following the initial decay is also reduced, resulting in a higher negative differential mobility cutoff frequency [11].

To complete the noise analysis, a plot of the PSD spatial distribution within the device is shown in Fig.4(b) at 100 GHz. As can be seen, the regions where the level of noise is the lowest are the regions where the carrier concentration is low (i.e. in the depleted region under the gate), or in the 2DEG where transport is almost free of scattering. The two peaks on the side coincide with the intersection of the electrode and the different type of semiconductor at the heterojunction. The n^+n regions created at this intersection generate an accumulation of charges responsible for the observed peaks. These peaks would disappear for a planar technology transistor design.

5 Conclusion

Based on recently published data [4], an AlInSb/InSb quantum well transistor has been modeled and simulated in this work, using full-band Monte Carlo simulations. A DC characterization was performed to extract the device current-voltage curves, showing a negative differential resistance behaviour for drain voltages above 1 V. A frequency analysis predicted a cutoff frequency

and a maximum frequency of oscillation of f_T = 500 GHz and f_{max} = 600 GHz, respectively. The authors believe these results are above what could be measured experimentally and offered explanations for this over estimated values. The noise analysis was performed also based on Monte Carlo simulations and allowed for a 2D identification of the noise within the device. Future work includes improving the device frequency behaviour analysis, and investigating the impact of scaling the device geometry on its small-signal representation.

6 Acknowledgements

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